Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application.

Listing of the Claims:

Claims 1-2 (canceled)

Claim 3 (currently amended): The system of claim ~~19~~ 22

wherein the sequential readout circuit determines a difference between ~~a final integration~~ the light ~~value~~ voltage and a reset ~~value~~ voltage for each photocell in the array in a time sequential manner.

Claim 4 (canceled)

Claim 5 (currently amended): The system of claim ~~19~~ 22 further comprising:

an integration capacitor having a first electrode for coupling to the input of the ~~single~~ amplifier and a second electrode for coupling to the output of the ~~single~~ amplifier; wherein the ~~single~~ amplifier includes a charge transfer mode and a unity gain mode.

Claim 6 (currently amended): The system of claim ~~19~~ 22 wherein the sequential readout circuit includes

a level shifting circuit that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode

coupled to the output terminal of the ~~single~~ amplifier for performing level shifting of the output of the ~~single~~ amplifier.

Claim 7 (currently amended): The system of claim ~~19~~ 22 wherein the sequential readout circuit includes

a gain manipulation circuit that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the ~~single~~ amplifier for performing gain manipulation of the ~~single~~ amplifier.

Claim 8 (currently amended): The system of claim ~~19~~ 22 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claim 9 (currently amended): The system of claim ~~19~~ 22 wherein the system is implemented in one of a scanner application, an optical mouse application, a video game controller application, a movement encoder application, a near field application, and a far field application.

Claim 10 (canceled)

Claim 11 (currently amended): The sequential readout circuit of claim ~~10~~ 23

wherein the ~~single~~ amplifier determines the difference between ~~a reset voltage (V_{reset}) and a light voltage (V_{light})~~ the light voltage and the reset voltage for the ~~first photocell and the second photocell~~ photocells in the array in a time sequential manner.

Claims 12-13 (canceled)

Claim 14 (currently amended): The sequential readout circuit of claim ~~10~~ 23

wherein the amplifier includes a charge transfer mode, a unity gain mode, a first input; and an output; and

wherein the circuit further includes an integration capacitor having a first electrode for coupling to the ~~first~~ negative input terminal and a second electrode for coupling to the output terminal of the amplifier.

Claim 15 (currently amended): The sequential readout circuit of claim ~~10~~ 23 further comprising:

a level-shifting mechanism that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing level shifting of the output of the amplifier.

Claim 16 (currently amended): The sequential readout circuit of claim ~~10~~ 23 further comprising:

a gain mechanism that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing gain manipulation of the amplifier.

Claim 17 (currently amended): The sequential readout circuit of claim ~~10~~ 23 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claim 18 (currently amended): The sequential readout circuit of claim ~~10~~ 23 wherein the sequential readout circuit is implemented in one of a scanner application, an optical mouse application, a video game controller application, a movement encoder application, a near field application, and a far field application.

Claims 19-21 (canceled)

Claim 22 (new): A system comprising:

a) an array of photocells that are arranged in rows and columns; and

b) a sequential readout circuit for sequentially reading out the value of the photocells one photocell at a time; wherein the sequential readout circuit includes

for each column

a sampling capacitor that includes a first electrode for coupling to a respective column and a second electrode, wherein the sampling capacitor measures the difference between the light voltage and the reset voltage generated by the photocells in the respective column; and

a switch that includes a first electrode coupled to the second electrode of the sampling capacitor, a second electrode, and a third electrode for receiving a sample control signal; wherein the switch selectively couples the first electrode of the switch to the second electrode of the switch when the sample control signal is asserted; and

an amplifier that includes a negative input terminal coupled to the second electrode of the switch; wherein the amplifier includes an output terminal for generating a voltage value that corresponds to the amount of light received by a particular photocell in the array.

Claim 23 (new): A sequential readout circuit for coupling to an array of photocells that includes a plurality of photocells that are arranged in rows and columns, each photocell generating a light voltage during a first period of time that represents received light and a reset voltage after being reset, the sequential readout circuit comprising:

for each column

a) a sampling capacitor that includes a first electrode for coupling to a respective column and a second electrode, wherein the sampling capacitor measures the difference between the light voltage and the reset voltage generated by the photocells in the respective column;

b) a switch that includes a first electrode coupled to the second electrode of the sampling capacitor, a second electrode, and a third electrode for receiving a sample control signal; wherein the switch selectively couples the first electrode of the switch to the second electrode of the switch when the sample control signal is asserted; and

c) an amplifier that includes a negative input terminal coupled to the second electrode of the switch; wherein the amplifier includes an output terminal for generating a voltage value that corresponds to the amount of light received by a particular photocell in the array.

Claim 24 (new): The sequential readout circuit of claim 23 wherein the sequential readout circuit sequentially reads out the value of the photocells one photocell at a time

Claim 25 (new): The system of claim 22 wherein the sampling capacitor measures the light voltage from a photocell, measures the reset voltage from a photocell, and stores a charge that represents the difference between the light voltage and the reset voltage.

Claim 26 (new): The sequential readout circuit of claim 23 wherein the sampling capacitor measures the light voltage from a photocell, measures the reset voltage from a photocell, and stores a charge that represents the difference between the light voltage and the reset voltage.